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Box: PATENT APPLICATION
Director of Patents and Trademarks
Washington, D.C. 20231

Attorney Reference: F98ED0762

Re: New Patent Application of: Hiroki NAKAMURA
Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Sir:

Please find attached hereto an application for patent which includes:

[x] Specification, Claims and Abstract (23 pages)
[x] 8 Sheets of Drawings (Fig. 1A through Fig. 8C)
[x] Inventor Declaration and Power of Attorney (3 Pages)
[x] Assignment document with cover page (2 Pages)
[x] Information Disclosure Statement, Form PTO-1449, and 2 references
[x] Claim for Priority and one (1) priority document – Japanese Patent Application No. 11-369811 filed December 27, 1999
[x] Preliminary Amendment

FEE CALCULATION

Basic Fee $345/690	$ 690.00
Additional Fees:	
Total number of claims: 26 in excess of 20: 6 times $09/18	$ 108.00
Number of independent claims: 3 in excess of 3: 0 times $39/78	$ 00.00
Multiple Dependent Claims $130/260	$ 00.00
Recording Fee $40.	$ 40.00
TOTAL FEES FOR THE ABOVE APPLICATION	**$ 838.00**

Please charge the fee to our Account No. 50-0945 and notify us accordingly.

The rights of priority are claimed under 35 USC §119 of Japanese Application No. 11-369811, filed December 27, 1999.

Respectfully submitted,

Junichi Mimura
Reg. No. 40,351

July 25, 2000
Date

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Hiroki NAKAMURA
Serial No.	: (not yet assigned)
Filed	: July 25, 2000
For	: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME
Attorney Ref.	: F98ED0762

PRELIMINARY AMENDMENT

Hon. Director of Patents and Trademarks
Washington, D.C. 20231

Sir:

Before examining the above-identified application, please amend the application as follows:

IN THE SPECIFICATION:

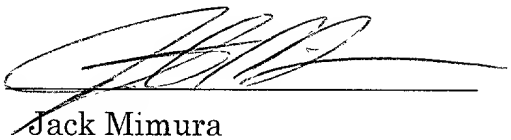
Page 1, line 15, change the figure number "9A" to --8A--.

Page 1, line 15, change the figure number "9C" to --8C--.

REMARKS

Examination on the merits is awaited.

Respectfully submitted,

By 

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July 25, 2000

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Japanese Patent Application No. 11-369811, filed December 27, 1999, the entire subject matter of which is incorporated herein of reference.

BACKGROUND OF THE INVENTION

1. Field of the invention

The invention relates to a semiconductor device, which has at least one dummy pattern to protect wiring patterns from corrosion.

2. Description of the related art

A semiconductor device having metalized wiring pattern in the related art is formed in the process described below with reference to Figs. 9A through 9C.

Referring to Fig. 8A, a semiconductor substrate 101 having circuit elements, such as transistors, in a circuit area of a chip area on its surface is prepared, and then, a metal layer which is formed of Aluminum are formed on the entire main-surface of the semiconductor substrate 101. Then, metalized wiring patterns 102 are formed by etching the metal layer to make an interconnection of the circuit elements.

Next, referring to Fig. 8B, a first insulating layer 103, such as a silicon oxide layer, is formed on the entire main-surface of the semiconductor substrate 101 and on

the exposed surface of the metalized wiring patterns 102 by the CVD process. After that, a SOG (Spin On Grass) layer 104 as a second insulating layer is coated on the first insulating layer 103 to planarized its surface. According to the spin coating process, the thick SOG layer is formed in an area where no wiring patterns is formed, and the thin SOG layer is formed on the wiring patterns. Then, a third insulating layer 105, such as a silicon oxide layer, is formed on the SOG layer by the CVD process.

After that, referring to Fig. 8C, the first insulating layer 103, the SOG layer 104, the third insulating 105 layer only in an grid line area is removed to make an opening 106 until the surface of the semiconductor is exposed. This process is very important to avoid cracking the semiconductor device at the scribing process.

However, as the SOG layer is exposed at an edge 1000 of the opening 106, moisture comes into the semiconductor device because the SOG layer has hygroscopicity. As a result, the metalized wiring patterns are corroded.

SUMMARY OF THE INVENTION

An objective of the invention is to resolve the above-described problem and to provide a semiconductor device having a dummy pattern to protect wiring patterns formed in the semiconductor device from corrosion.

The objective is achieved by a semiconductor device including a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area, circuit patterns formed on the substrate in the circuit area, a first dummy pattern which is formed of the same

material as the circuit pattern, formed in the dummy area, the dummy pattern encompassing the circuit area, a first insulating layer formed on an entire surface of the semiconductor substrate, a second insulating layer formed only on the first insulating layer which is formed on the semiconductor substrate and on the circuit patterns; and a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

The objective is further achieved by a method for manufacturing a semiconductor device including a step for preparing a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area, a step for forming a conductivity layer on the semiconductor substrate, a step for forming circuit patterns in the circuit area and a dummy pattern encompassing the circuit area in the dummy area by etching the conductivity layer, a step for forming a first insulating layer formed on an entire surface of the semiconductor substrate, a step for forming a second insulating layer on the first insulating layer, a step for removing the second insulating layer which is formed on the first insulating layer on the dummy pattern until the surface of the first insulating layer is exposed, a step for forming a third insulating layer formed on the exposed first insulating layer and on the second insulating layer; and , a step for removing the first, second and third insulating layers in the grid-line area.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more particularly described with reference to the accompanying drawings in which:

Figs. 1A through 1C are sequential sectional views for forming a semiconductor device of a first of fifth illustrative embodiments of the invention;

Fig. 2A is a graph showing a relationship between the thickness of a SOG layer formed on the dummy pattern and the width (Lw) of the dummy pattern or the length (LS) between the dummy pattern and metalized wiring pattern, of the first embodiment;

Fig. 2B is an enlarged sectional view at the edge of the circuit area to indicate the width (Lw) and the length (Ls1) which is used in Fig. 2A;

Figs. 3A through 3C are sequential sectional views for forming a semiconductor device of a second of fifth illustrative embodiments of the invention;

Fig. 4A is a graph showing a relationship between the thickness of a SOG layer formed on the second dummy pattern and the width (Lw) of the second dummy pattern or the length (Ls1) between the second dummy pattern and metalized wiring pattern, of the second embodiment;

Fig. 4B is an enlarged sectional view at the edge of the circuit area to indicate the width (Lw) and the length (Ls1) which is used in Fig. 4A

Figs. 5A through 5E are sequential sectional views for forming a semiconductor device of a third of fifth illustrative embodiments of the invention;

Fig. 6 is a sectional view of a semiconductor device of a fourth of fifth illustrative

embodiments of the invention;

Fig. 7a is a sectional view of a semiconductor device of a fifth of fifth illustrative embodiments of the invention;

Fig. 7b is a enlarged plan view of the semiconductor device shown in Fig, 7a; and

Figs. 8A through 8C are sequential sectional views for forming a semiconductor device in the related art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 1A, unillustrated circuit elements, such as transistors, are formed in a circuit area of the chip area on a main-surface of the semiconductor substrate 201, and then, an unillustrated insulating layer is formed on the surface of the semiconductor substrate 201. Next, a metal layer having a thickness of 600nm, which is formed of Aluminum, is formed on the entire main-surface of the semiconductor substrate 201, and then, metalized wiring patterns 202 are formed in the circuit area by etching the metal layer to make an interconnection of the circuit elements. Simultaneously, a dummy pattern 202a, which is electrically isolated from the wiring pattern 202, is formed in a dummy area by etching the metal layer. The dummy area is disposed between the circuit area and the grid-line area. A manufacturing margin area is located on either side of the dummy area from the circuit area and grid-line area, respectively. For example, a frame-shaped dummy area having a width of ((1000-0.05)-(800+0.05))/2 μm is formed, providing that the chip

area has 1000 X 1000 μm, the circuit area whose center is correspondence to a center of the chip area, has 800 X 800 μm, and width of the manufacturing margin is 0.05 μm. Therefore, the circuit area is encompassed with the dummy area. Although the dummy pattern 202a can be formed in the dummy area, preferably, the distance (L) between the edge 1000 of the chip area and an outer edge of the dummy pattern 202a is set for over 10 μm.

Next, referring to Fig. 1B, a first insulating layer 203, such as silicon oxide layer, having a thickness of 200nm is formed by CVD on the entire surface of the semiconductor substrate 201. Then, a SOG layer 204 as a second insulating layer is coated only on the first insulating layer 203 which is directly formed on the semiconductor substrate 201 and which is formed on the metalized wiring patterns 202 to planarize the surface. That is, the SOG layer is not formed on the first insulating layer 203, which is formed on the dummy pattern 202a. The condition not to be formed the SOG layer on the dummy pattern is explained later. Then, a third insulating layer 205 having a thickness of 400nm is formed by CVD on the SOG layer 204 and the exposed first insulating layer 203 which is formed on the dummy pattern 202a.

Then, referring to Fig. 1C, the first insulating layer 203, the SOG layer 204, and the third insulating layer 205 on the grid line area are removed until the surface of the semiconductor substrate 201 is exposed.

In the process shown in Fig. 1B, the SOG layer is coated in the following condition and the thickness of the SOG layer 204 on the dummy pattern 202a is

measured in changing the width (Lw) of the dummy pattern 202a or the length (Ls1) between the dummy pattern 202a and metalized wiring pattern 202. A result of the measurement is shown in Fig. 2A.

(1) the material of the SOG layer: Concentration of Solid content is 5.2wt%

(2) the material of the SOG layer: Viscosity is 1.03 mPa.sec.

(3) Rotary speed: 5000 rpm

Referring to Figs. 2A and 2B, the X axis shows the thickness of the SOG layer on the dummy pattern 202a, and Y axis shows the width (Lw) of the dummy pattern 202a or length (Ls1) between the dummy pattern 202a and metalized wiring pattern 202.

In Fig. 2A, the black circles shows the relationship between the thickness of the SOG layer and the width (Lw) of the dummy pattern 202a where the length (Ls1) is fixed to 2.6 μm and the width (Lw) is changed from 1 to 100 μm. In this case, it is found that if the width (Lw) is getting wider, the SOG layer becomes thicker. The with circles shows the relationship between the thickness of the SOG layer and the length (Ls1) where the width (Lw) is fixed to 1.0 μm and the length (Ls1) is changed from 0.9 to 5 μm. In this case, it is found that the thickness of the SOG layer on the dummy pattern 202a is maintained to nearly zero even if the length (Ls1) is set until 5 μm.

As a result form this experimentation, if the width (Lw) is designed to 1.0 μm, the SOG layer is not formed on the dummy pattern 202a. Therefore, if the dummy pattern 202a having a width of 1.0 μm is formed, the SOG layer 204 which is adjacent

to the grid-line area is completely isolated from the SOG layer 204 which is formed in the circuit area by the first insulating layer 203 formed on the dummy pattern 203.

According to the first embodiment of the invention, as the SOG layer 204 which is adjacent to the grid-line area is completely isolated from the SOG layer 204 which is formed in the circuit area by the first insulating layer 203 formed on the dummy pattern 203, it is possible to protect the semiconductor device from moisture which comes into the semiconductor device through the SOG layer 204. Further, as the dummy pattern 202a can be formed with the metalized wiring patterns, simultaneously, it is not necessary to add some additional process. Furthermore, since the dummy pattern is formed outside of the circuit area, the surface of the semiconductor device at the peripheral area is planarized as the additional effect of the dummy pattern.

The second embodiment is described below with reference to Figs. 3A through 3C and Figs. 4A through 4B. Referring to Fig. 3A, unillustrated circuit elements, such as transistors, are formed in a circuit area of the chip area on a main-surface of the semiconductor substrate 201, and then, an unillustrated insulating layer is formed on the surface of the semiconductor substrate 201. Next, a tungsten polycide layer having a thickness of about 3000 μm is formed on the insulating layer, and then, a lower dummy pattern 300a (a second dummy pattern) is formed in a dummy area by etching the tungsten polycide layer. As well as the dummy area decried in the first embodiment, the dummy area of the second embodiment is disposed between the circuit area and the grid-line area. A manufacturing margin area is located on either side of the dummy area from the circuit area and grid-line area, respectively. Further,

as well as the first dummy patterns 202a in the first embodiment, the lower dummy pattern 300a of the second embodiment having the width (Lw) can be formed anywhere in the dummy area, preferably, the distance (L) between the edge 1000 of the chip area and an outer edge of the lower dummy pattern 300a is set for over 10 μm. Also, the circuit area is encompassed with the lower dummy pattern 300a. Next, a borophosphosilicate glass (BPSG) layer 302 having a thickness of 800nm is formed on the silicon substrate and the lower dummy pattern 300a. The impurity concentrations of P2O5 and B2O3 in BPSG layer are 15wt% and 10wT%, respectively. Then, a thermal treatment is performed to the BPSG layer 302 for thirty minutes at 900 C in the nitrogen atmosphere to planarize its surface. After that, an aluminum layer having a width of 600nm is formed on the BPSG layer 302, and then, metalized wiring patterns 304 are formed in the circuit area by etching the metal layer to make an interconnection of the circuit elements. Simultaneously, an upper dummy pattern 304a (first dummy pattern), which is electrically isolated from the wiring pattern 304, is formed above the lower dummy pattern 300a. The shape and side of the upper dummy pattern 304a are almost the same as the lower dummy pattern 302a.

Next, referring to Fig. 3B, a first insulating layer 306, such as silicon oxide layer, having a thickness of 200nm is formed by CVD on the surface of the BPSG layer 302, on the surface of metalized wiring patterns 304 and on the upper dummy pattern 304a. Then, a SOG layer 308 as a second insulating layer is coated only on the first insulating layer 306 which the lower dummy pattern 300a is not formed thereunder to planarize the surface. That is, the SOG layer is not formed on the first insulating

layer 306 which is formed on the upper dummy pattern 304a. The condition not to be formed the SOG layer on the upper dummy pattern 304a is explained later. Then, a third insulating layer 310 having a thickness of 400nm is formed by CVD on the SOG layer 308 and on the exposed first insulating layer 306 which is formed on the upper dummy pattern 304a.

Then, referring to Fig.3C, the first insulating layer 306, the SOG layer 308, and the third insulating layer 310 on the grid line area are removed until the surface of the BPSG layer 302 is exposed.

In the process shown in Fig. 3B, the SOG layer 308 is coated in the following condition and the thickness of the SOG layer 308 on the upper dummy pattern 304a is measured in changing the width (Lw) of the lower and upper dummy pattern 302a, 304a or the length (Ls1) between the lower and upper dummy pattern 302a, 304a and metalized wiring pattern 304. A result of the measurement is shown in Fig. 4A.

(4) the material of the SOG layer: Concentration of Solid content is 5.2wt%

(5) the material of the SOG layer: Viscosity is 1.03 mPa.sec.

(6) Rotary speed: 5000 rpm

Referring to Figs. 4A and 4B, the X axis shows the thickness of the SOG layer on the upper dummy pattern 304a, and Y axis shows the width (Lw) of the lower and upper dummy pattern 302a, 304a or length (Ls1) between the lower and upper dummy pattern 302a, 304a and metalized wiring pattern 304.

In Fig. 4A, the black circles shows the relationship between the thickness of the SOG layer and the width (Lw) of the lower and upper dummy pattern 302a, 304a

where the length (Ls1) is fixed to 2.6 μm and the width (Lw) is changed from 1 to 7 μm. In this case, it is found that the SOG layer becomes thicker if the width (Lw) is designed for over 2 μm,. The with circles shows the relationship between the thickness of the SOG layer and the length (Ls1) where the width (Lw) is fixed to 1.0 μm and the length (Ls1) is changed from 0.9 to 5 μm. In this case, it is found that the thickness of the SOG layer on the second dummy pattern 304a is maintained to nearly zero even if the length (Ls1) is designed until 5 μm.

As a result form this experimentation, if the width (Lw) is set to 1 μm – 2 μm the SOG layer is not formed on the upper dummy pattern 304a. Therefore, if the upper dummy pattern 304a having a width of 1 μm – 2 μm is formed, the SOG layer 308 which is adjacent to the grid-line area is completely isolated from the SOG layer 308 which is formed in the circuit area by the first insulating layer 306 formed on the upper dummy pattern 304a.

According to the second embodiment of the invention, in addition to the benefits of the first embodiment, the following advantages can be obtained.

Although the material of the lower dummy pattern 302a is not limited for the metal such as tungsten polycide, if it is formed of the conductivity material, metalized wiring patterns can be formed with the lower dummy pattern 302a. Further, the second embodiment of the invention can be adapted to any semiconductor device having multi-wiring layers without any additional processes. Furthermore, as the width (Lw) of the lower and upper dummy pattern 302a, 304a can be designed with a

range from 1 μm to 2 μm, it becomes easier to design the total semiconductor device.

The third embodiment is described below with reference to Figs. 5A through 5D. Referring to Fig. 5A, unillustrated circuit elements, such as transistors, are formed in a circuit area of the chip area on a main-surface of the semiconductor substrate 201, and then, an unillustrated insulating layer is formed on the surface of the semiconductor substrate 201. Next, a metal layer which, is formed of Aluminum, is formed on the entire main-surface of the semiconductor substrate 201, and then, metalized wiring patterns 402 are formed in the circuit area by etching the metal layer to make an interconnection of the circuit elements. Simultaneously, a first dummy pattern 402a, which is electrically isolated from the wiring pattern 402, is formed in a dummy area by etching the metal layer. As well as in the first and second embodiment, the dummy area is disposed between the circuit area and the grid-line area. A manufacturing margin area is located on either side of the dummy area from the circuit area and grid-line area, respectively. Further, as well as in the first embodiment, the first dummy pattern 402a of the third embodiment having the width (Lw) can be formed anywhere in the dummy area, preferably, the distance (L) between the edge 1000 of the chip area and an outer edge of the first dummy pattern 402a is set for over 10 μm. Also, the circuit area is encompassed with the first dummy pattern 402a.

Next, referring to Fig. 5B, a first insulating layer 404, such as silicon oxide layer, having a thickness of 200nm is formed by CVD on the entire surface of the semiconductor substrate 201. Then, a multi-SOG layer 406 as a second insulating

layer is formed on the first insulating layer 404 to planarize its surface. The multi-SOG layer 406 is formed by coating a SOG layer few times. That is, a first SOG layer is coated on the first insulating layer 404. Then, after it is dried up, a second SOG layer is coated on the dried SOG layer.

Next, referring to Fig. 5C, the multi-SOG layer is etched by the well-known RIE method under the conditions below until the surface of the first insulating layer 404 on the first dummy pattern 402a is exposed.

(a) Gas flow rate: CHF3/CF4/Ar = 20/15/200 [sccm]

(b) Pressure: 40 [Pa]

(c) RF power: 200 [W]

(d) Etching rate of the multi-SOG layer: 7.5 [nm/sec]

Next, referring to Fig. 5D, the third insulating layer 408 having a thickness of 400nm is formed by CVD on the multi-SOG layer 406 and the exposed first insulating layer 404 which is formed on the first dummy pattern 402a..

Then, referring to Fig. 5E, the first insulating layer 404, the multi-SOG layer 406, and the third insulating layer 408 on the grid line area are removed until the surface of the semiconductor substrate 201 is exposed.

According to the third embodiment of the invention, in addition to the benefits of the first embodiment, the following advantages can be obtained. In the first and second embodiments, the SOG layer can not be formed thick. If it were formed thick, it would be formed on the first insulating layer on the first dummy pattern. However, as the multi-SOG layer can be formed thick in the third embodiment, the planarized

surface can be obtained in the circuit area.

The fourth embodiment is described below with reference to Fig. 7. Referring to Fig. 7, a pair of inner and outer dummy patterns 500a, 500b (a third dummy pattern and a first dummy pattern) are formed in the dummy area. Each dummy pattern has a same width (Lw), and formed in the same method with the same size described in the first embodiment. The length (Ls2) between the dummy patterns 500a, 500b is designed for over 0.9 μm.

According to the fourth embodiment, in addition to the benefits of the first embodiment, the following advantages can be obtained.

Even If the SOG layer 504 is formed on the first insulating layer 502 on the outer dummy pattern 500b by accident, the semiconductor device can be protected from the moisture because the SOG layer 504 formed on the outer dummy pattern 500b is isolated from the SOG layer 504 formed in the circuit are by the insulating layer formed on the inner dummy pattern 500a.

The fifth embodiment is described below with reference to Figs. 7A and 7B. A bonding pad 601 is formed in a circuit area, and an outer dummy pattern 600a (a first dummy pattern) is formed in a dummy area. The size, location and manufacturing process of the outer dummy pattern is the same as the dummy pattern described in the first embodiment. That is, a width of the outer dummy pattern is designed for 1 μm, and the length (L) is designed for 10 μm. A frame-shaped fourth dummy pattern 600b is formed for surrounding the bonding pad 601 in the circuit area. The distance (Ls3) between the bonding pad 601 and the fourth dummy pattern 600b or

the outer dummy pattern 600a is designed for over 0.9 μm. The distance (Ls1) between the metalized wiring pattern 600 and the outer dummy pattern 600a or the fourth dummy pattern is designed for over 0.5 μm because of the same reason described in the first embodiment. The metalized wiring pattern 600, the outer dummy pattern 600b and the fourth dummy pattern 600a are formed simultaneously by etching a conductive layer.

According to the fifth embodiment, in addition to the benefits of the first embodiment, the following advantages can be obtained. As the bonding pad 601 is surrounded by the fourth dummy pattern 600a, an SOG layer 606, which is exposed to an opening 602 for the bonding pad 601 is isolated to the SOG layer 606 which is formed in the circuit area. Therefore, it is possible to protect the semiconductor device from moisture which comes into the semiconductor device through the SOG layer 204 exposed to the opening 602.

While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. For example, although silicon oxide layers are used for the first and third insulating layer in the first through fifth embodiment, a silicon nitride layer, a PSG layer, a BPSG layer can be used. Further, it is possible to change the width of the dummy patterns in the first through fifth embodiment based on the concentration of solid content of the SOG layer. If a high concentrate material for the SOG layer is used, the dummy pattern having a wide width may be formed. On the contrary, If a low concentrate material for the SOG layer is used, the dummy pattern having a short width may be formed. Also,

in the third embodiment, it is possible to change the etching time based on the concentration of solid content of the SOG layer. Furthermore, in the second embodiment, the BPSG layer can be changed to other layer having thermal plagiarizing characteristics, such as a PSG layer. Various modifications of the illustrated embodiments, as well as other embodiments of the invention, will be apparent to those skilled in the art on reference to this description. Therefore, the appended claims are intended cover any such modifications or embodiments as fall within the true scope of the invention.

What I claim is:

1. A semiconductor device, comprising:

a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area;

circuit patterns formed on the substrate in the circuit area;

a first dummy pattern which is formed of the same material as the circuit pattern, formed in the dummy area, the dummy pattern encompassing the circuit area;

a first insulating layer formed on an entire surface of the semiconductor substrate;

a second insulating layer formed only on the first insulating layer which is formed on the semiconductor substrate and on the circuit patterns; and

a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

2. A semiconductor device as claimed in claim 1, wherein the second insulating layer is a SOG layer.

3. A semiconductor device as claimed in claim 2, wherein the width of the first dummy pattern is fixed by a concentration of solid content of the SOG.

4. A semiconductor device as claimed in claim 1, wherein the width of the first dummy pattern is designed for less 1 μm where a concentration of solid content of the

SOG is around 5.2 wt%.

5. A semiconductor device as claimed in claim 1, further comprising,

a second dummy patter formed under the first dummy pattern; and

a fourth insulating layer formed directly on the substrate and on the second dummy layer, the fourth insulating layer having characteristics that its surface is planarized by a thermal treatment,

whereby, the first dummy pattern is formed on the fourth insulating layer which is formed on the first dummy layer, and the circuit patterns are formed on the fourth insulating layer.

6. A semiconductor device as claimed in claim 5, wherein a shape and size of the second dummy pattern is almost the same as these of the first dummy pattern.

7. A semiconductor device as claimed in claim 5, wherein the fourth insulating layer is BPSG layer.

8. A semiconductor device as claimed in claim 5, wherein the second insulating layer is a SOG layer.

9. A semiconductor device as claimed in claim 6, wherein the widths of the first and second dummy patterns are fixed by a concentration of solid content of the SOG.

10. A semiconductor device as claimed in claim 6, wherein the widths of the first and second dummy patterns are designed for less 1 μm where a concentration of solid content of the SOG is around 5.2 wt%.

11. A semiconductor device as claimed in claim 1, further comprising,

a third dummy pattern formed between the first dummy pattern and the circuit area, the first insulating layer being not formed on the third dummy pattern.

12. A semiconductor device as claimed in claim 11, wherein a width of the third dummy pattern is almost the same as that of the first dummy pattern.

13. A semiconductor device as claimed in claim 11, wherein the distance between the first dummy pattern and the second dummy pattern is designed for over 0.9 μm.

14. A semiconductor device as claimed in claim 12, wherein the widths of the first and third dummy patterns are fixed by a concentration of solid content of the SOG.

15. A semiconductor device as claimed in claim 12, wherein widths of the first and third dummy patterns are designed for less 1 μm where a concentration of solid content of the SOG is around 5.2 wt%.

16. A semiconductor device as claimed in claim 1, further comprising,

a bonding pad formed on the semiconductor substrate in the circuit area;

a fourth dummy pattern surrounding the bonding pad, the first insulating layer being not formed on the fourth dummy pattern.

17. A semiconductor device as claimed in claim 16, wherein a width of the fourth dummy pattern is almost the same as that of the first dummy pattern.

18. A semiconductor device as claimed in claim 16, wherein a distance between the fourth dummy pattern and the bonding pad is designed for over 0.9 μm.

19. A semiconductor device as claimed in claim 17, wherein the widths of the first and fourth dummy patterns are fixed by a concentration of solid content of the SOG.

20. A semiconductor device as claimed in claim 117, wherein widths of the first and fourth dummy patterns are designed for less 1 μm where a concentration of solid content of the SOG is around 5.2 wt%.

21. A method for manufacturing a semiconductor device, comprising,

preparing a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area;

forming a conductivity layer on the semiconductor substrate;

forming circuit patterns in the circuit area and a dummy pattern encompassing the circuit area in the dummy area by etching the conductivity layer;

forming a first insulating layer formed on an entire surface of the semiconductor substrate;

forming a second insulating layer formed only on the first insulating layer which is formed on the semiconductor substrate and on the circuit patterns;

forming a third insulating layer formed on the exposed first insulating layer and the second insulating layer; and

removing the first, second and third insulating layers in the grid-line area.

22. A method for manufacturing a semiconductor device as claimed in claim 21, wherein the second insulating layer is formed by a SOG method.

23. A method for manufacturing a semiconductor device, comprising,

preparing a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area;

forming a conductivity layer on the semiconductor substrate;

forming circuit patterns in the circuit area and a dummy pattern encompassing the circuit area in the dummy area by etching the conductivity layer;

forming a first insulating layer formed on an entire surface of the semiconductor substrate;

forming a second insulating layer on the first insulating layer;

removing the second insulating layer which is formed on the first insulating layer on the dummy pattern until the surface of the first insulating layer is exposed;

forming a third insulating layer formed on the exposed first insulating layer and on the second insulating layer; and

removing the first, second and third insulating layers in the grid-line area.

24. A method for manufacturing a semiconductor device as claimed in claim 23, wherein the second insulating layer is formed by a SOG method.

25. A method for manufacturing a semiconductor device as claimed in claim 23, wherein the second insulating layer is removed by a RIE method.

26. A method for manufacturing a semiconductor device as claimed in claim 23, wherein the second insulating layer is a multi-SOG layer.

ABSTRACT

A semiconductor device including a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area, circuit patterns formed on the substrate in the circuit area, a first dummy pattern which is formed of the same material as the circuit pattern, formed in the dummy area, the dummy pattern encompassing the circuit area, a first insulating layer formed on an entire surface of the semiconductor substrate, a second insulating layer formed only on the first insulating layer which is formed on the semiconductor substrate and on the circuit patterns; and a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

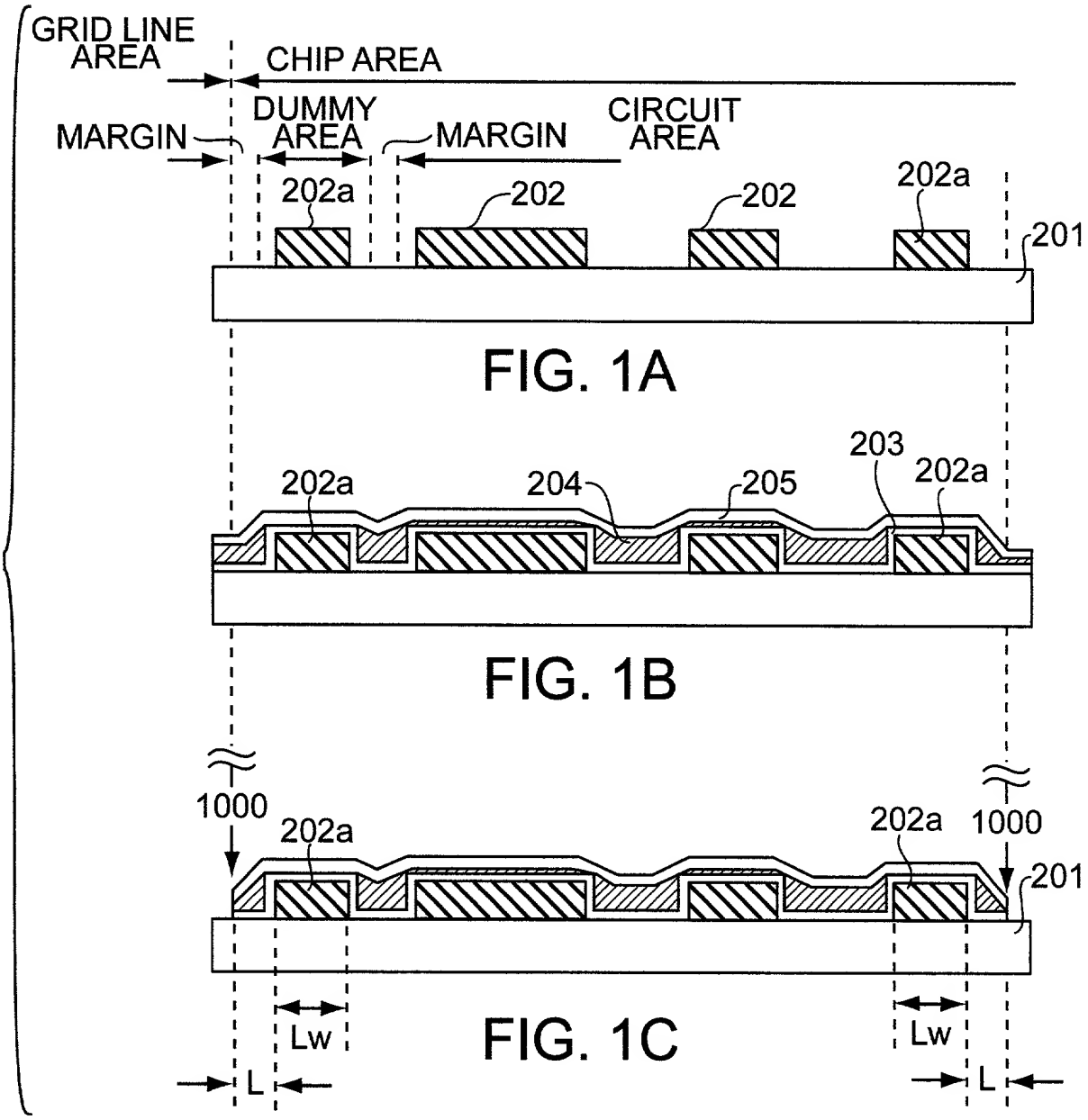

FIG. 1A

FIG. 1B

FIG. 1C

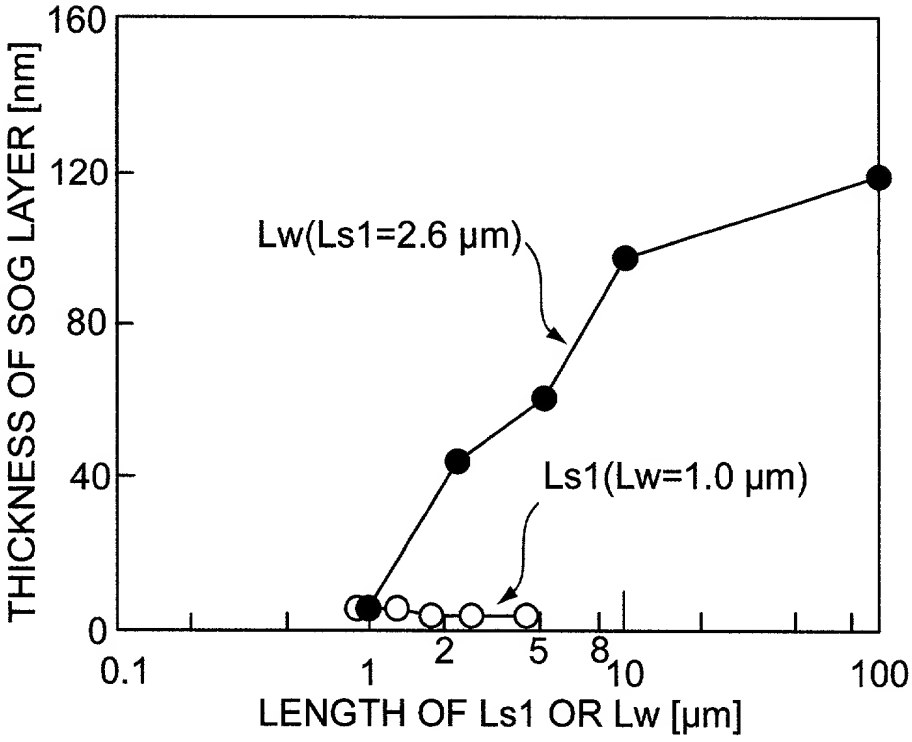
160
120
80
40
0
THICKNESS OF SOG LAYER [nm]
Lw(Ls1=2.6 μm)
Ls1(Lw=1.0 μm)
0.1
1
2
5
8
10
100
LENGTH OF Ls1 OR Lw [μm]

FIG. 2A

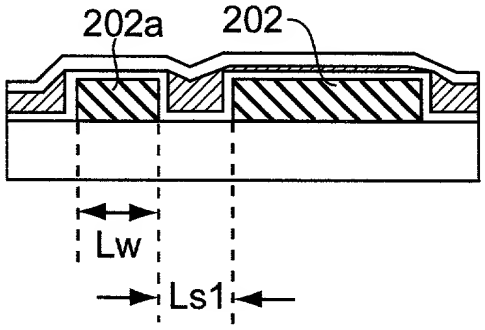
202a
202
Lw
Ls1

FIG. 2B

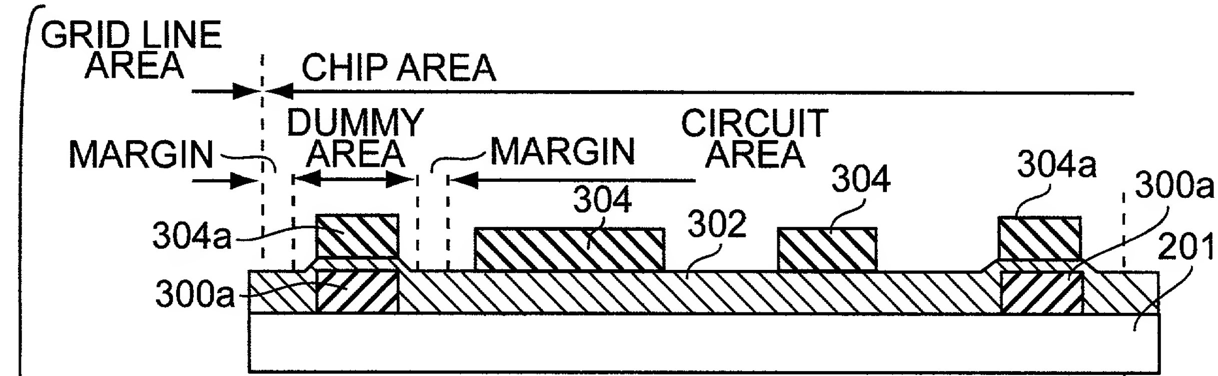

FIG. 3A

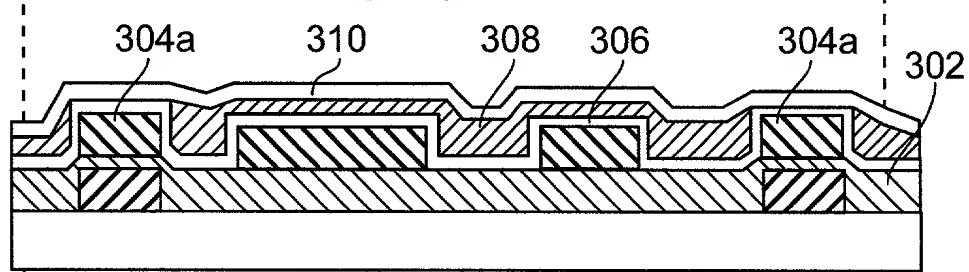

FIG. 3B

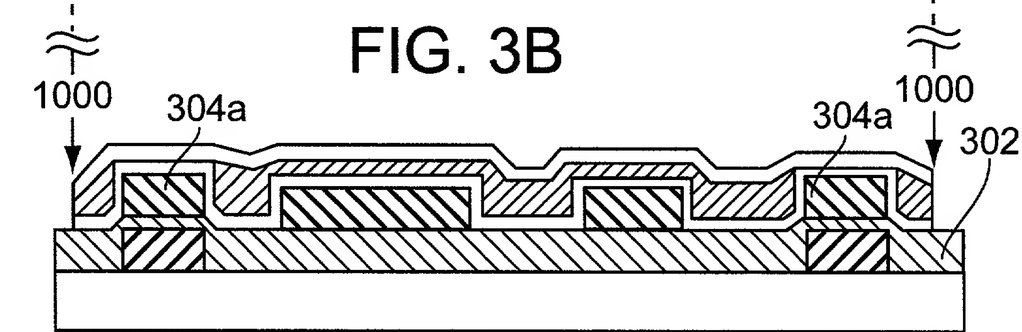

FIG. 3C

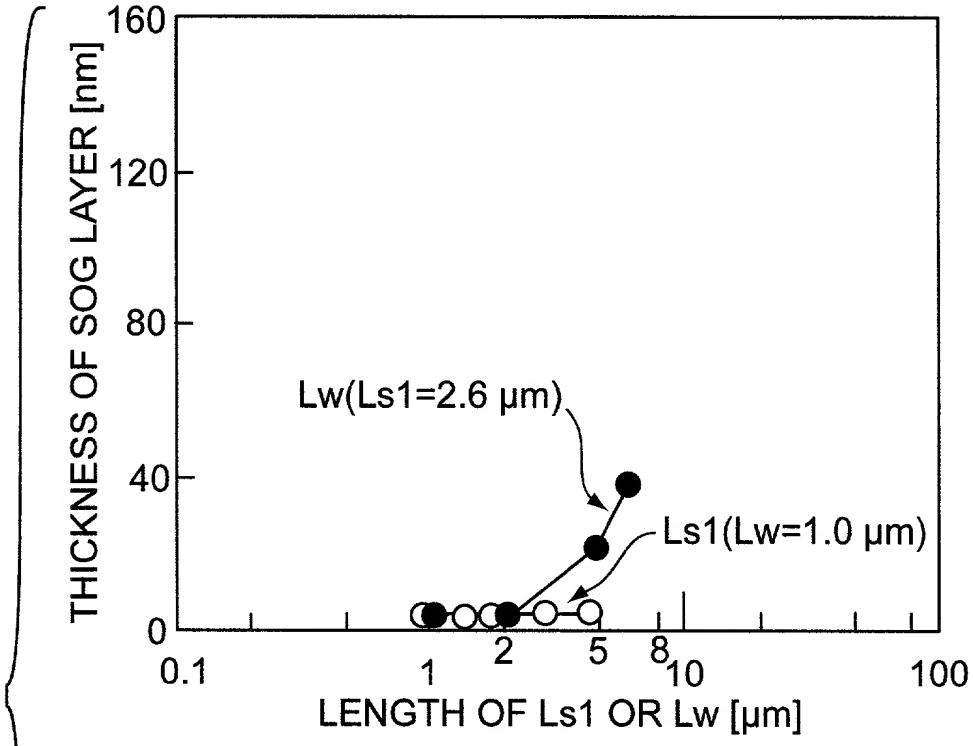
160
120
80
40
0
THICKNESS OF SOG LAYER [nm]
Lw(Ls1=2.6 μm)
Ls1(Lw=1.0 μm)
0.1
1
2
5
8
10
100
LENGTH OF Ls1 OR Lw [μm]

FIG. 4A

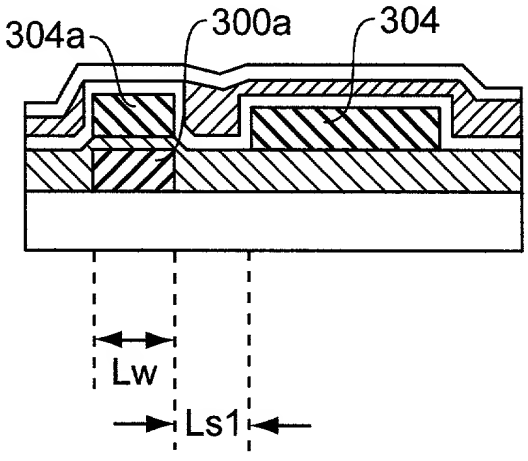
304a
300a
304
Lw
Ls1

FIG. 4B

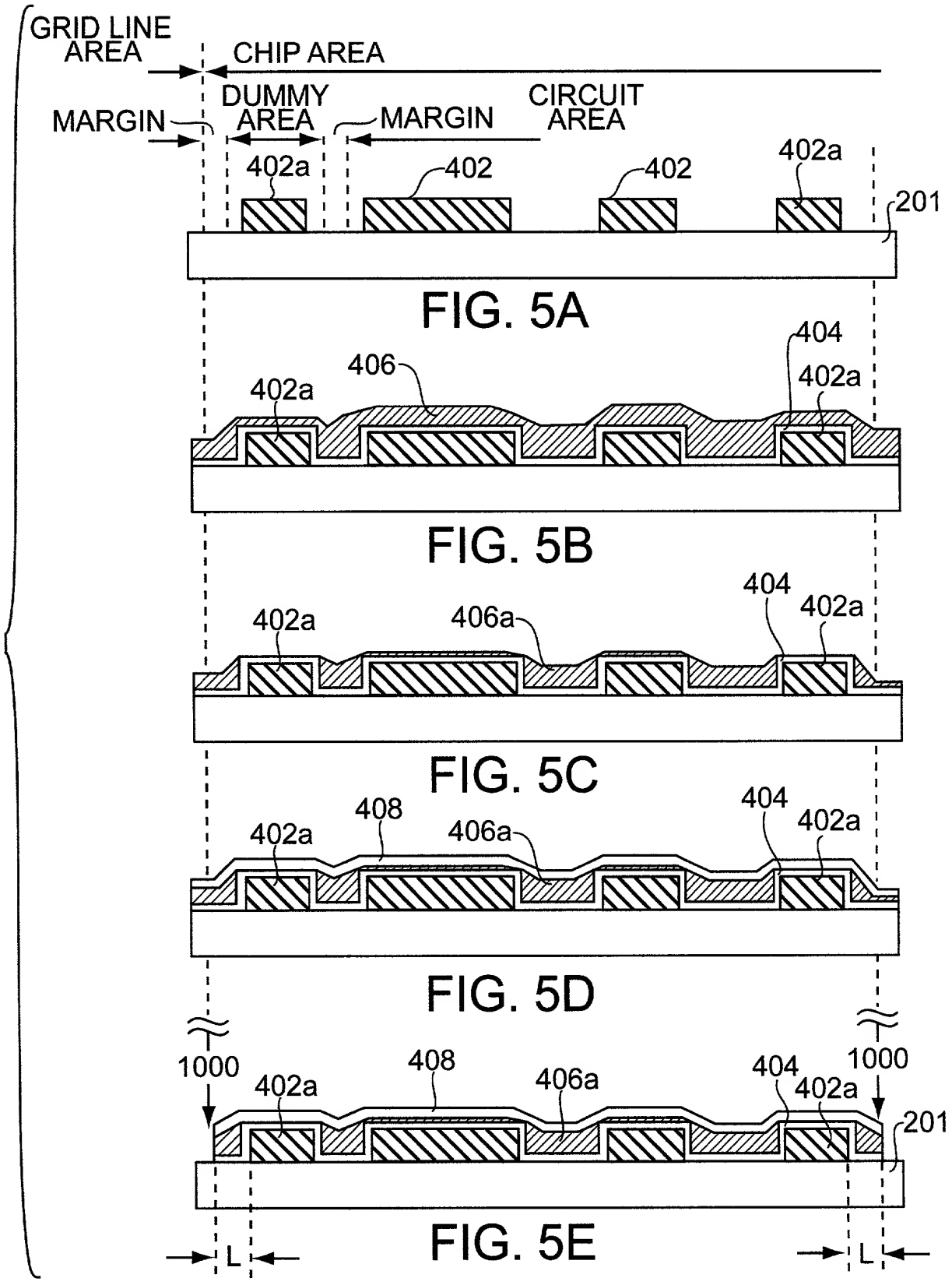

FIG. 5A

FIG. 5B

FIG. 5C

FIG. 5D

FIG. 5E

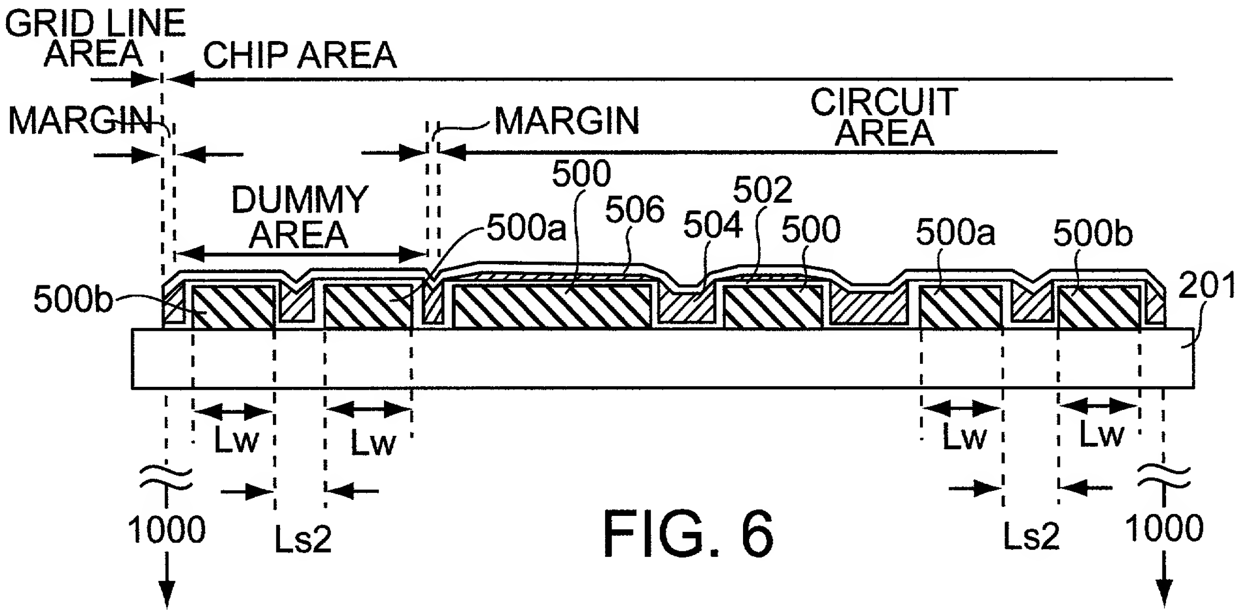

FIG. 6

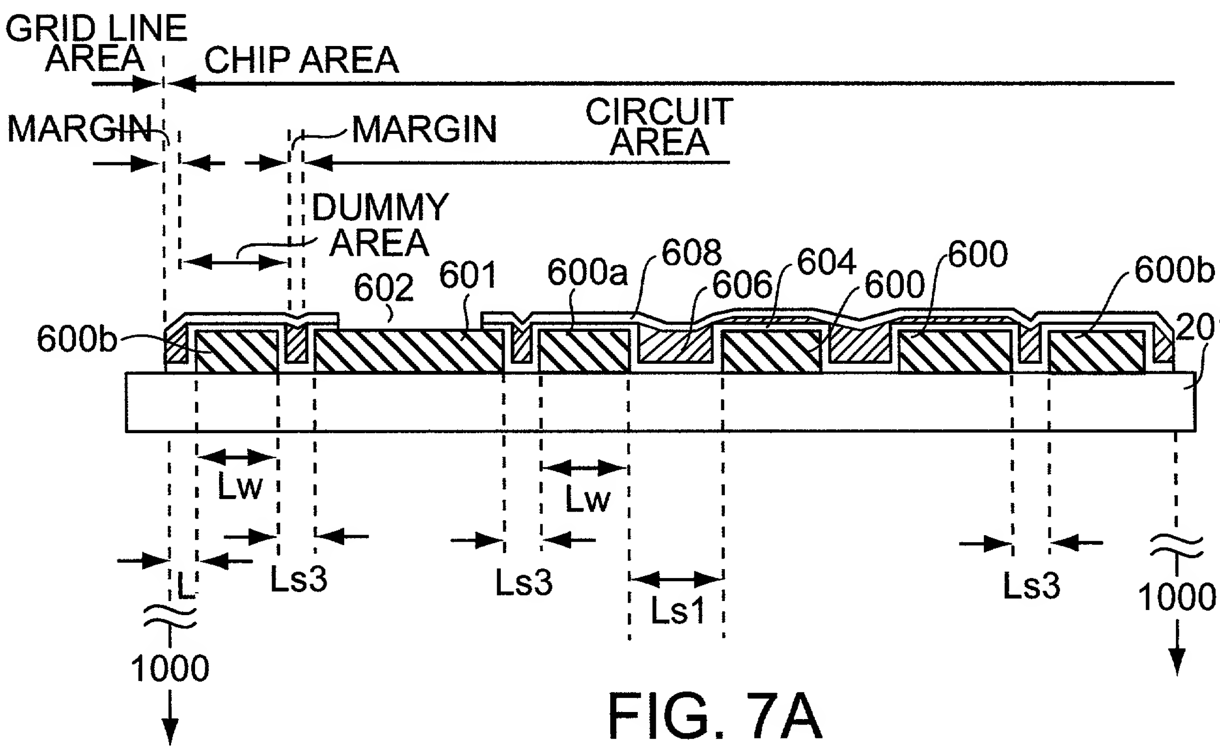

FIG. 7A

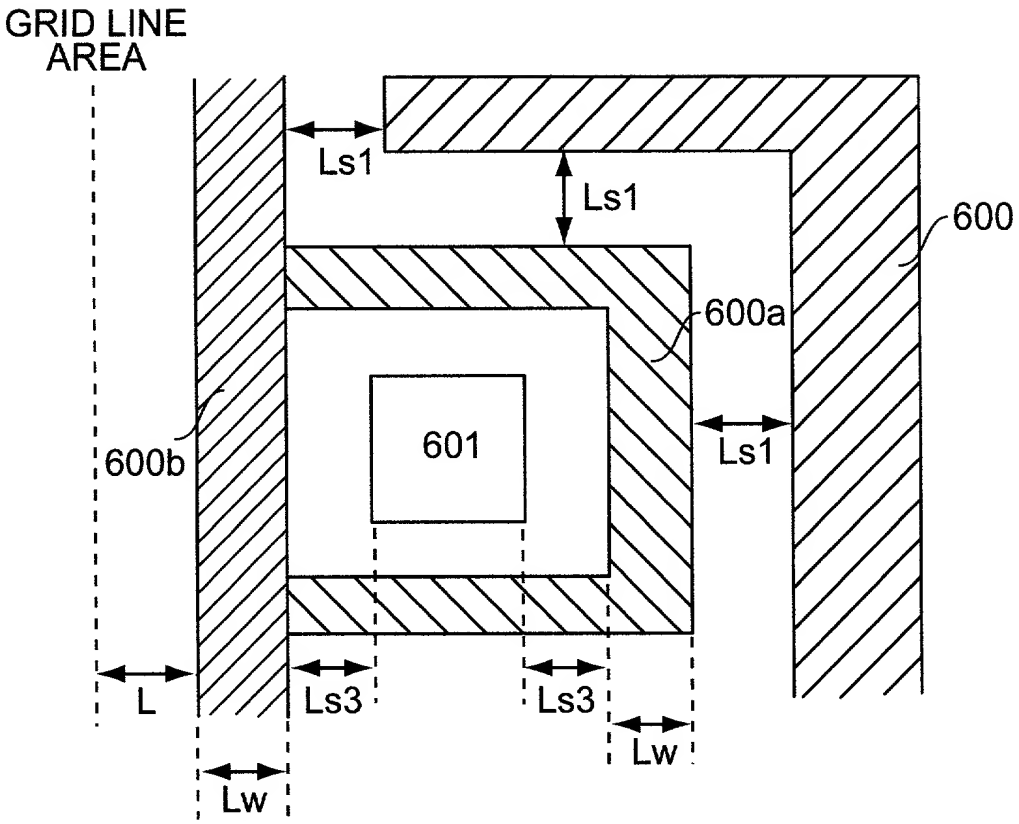

FIG. 7B

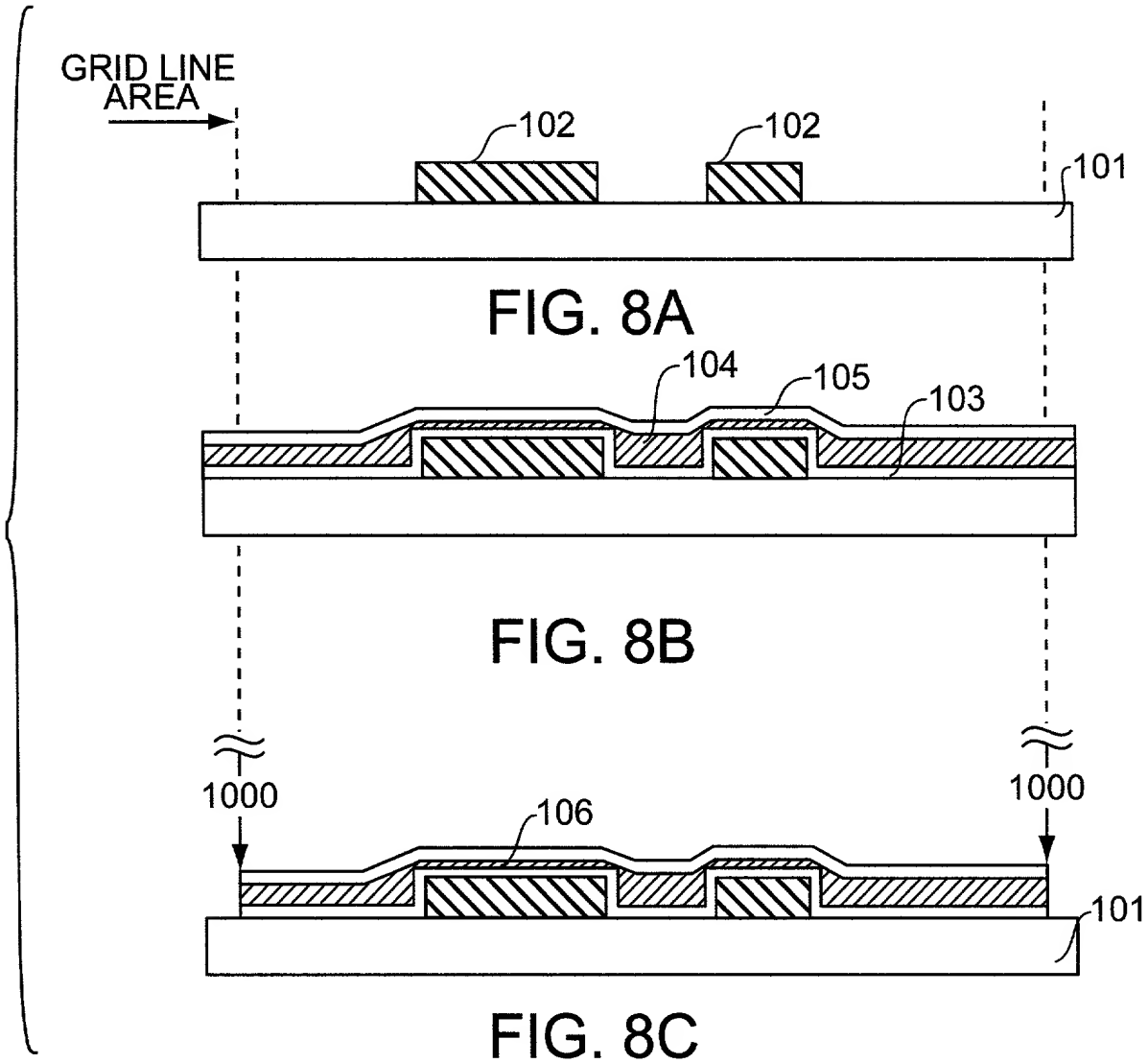

FIG. 8A

FIG. 8B

FIG. 8C

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Declaration and Power of Attorney For Patent Application
特許出願宣言書及び委任状
Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name

下記の名称の発明に関して請求範囲に記載され、特許出願している発明の内容について、私が最初かつ唯一の発明者（下記氏名が一つの場合）、もしくは最初かつ共同発明者であると（下記の名称か複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

半導体装置およびその製造方法

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked

☐ __ 月 __ 日に提出され、米国出願番号または特許協定条約国際番号を _____ とし、
（該当する場合）_____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable)

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above

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Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
11-369811	Japan	27/12/1999	☐
			☐

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(Application No) (出願番号)	(Filing Date) (出願日)

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(Application No) (出願番号)	(Filing Date) (出願日)	(Status Patented, Pending Abandoned) (現況 . 特許許可済、係属中、放棄済)
		(Status. Patented, Pending, Abandoned) (現況 特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made or information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statement and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

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POWER OF ATTORNEY As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number*

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第二共同発明者	Full name of second joint inventor, if any
第二共同発明者の署名　日付	Second inventor's signature　Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address
(第三以降の共同発明者に付いても同様に記載し、署名をすること)	(Supply similar information and signature for third and subsequent joint inventors)